Efficient Switching Pattern for Cascaded H-bridge Multilevel Inverter employing Series-connected Input Voltage Sources

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ABSTRACT: A multilevel inverter configuration which is designed by insertion of a bidirectional switch between capacitive voltage sources and a conventional H-bridge module can produce better sinusoidal waveform by increasing the number of output voltage levels. There are 24 basic switching patterns with the 9 output voltage levels. Among the patterns, we select 2 best efficient switching patterns to get lower switching loss and minimum *dv/dt* stress. And then we analyze characteristics of Total Harmonic Distortion (THD) of the output voltage with variation of input voltage. With appropriate switching pattern 1, we can utilize it to solar power system which has merit in the independent voltage source.

1 INTRODUCTION

Cascaded H-bridge multilevel inverter has been researched for high voltage applications since it has advantages in number of components, high reliability, and modularity. The general purpose of multilevel inverter is a generation of a high voltage using lower voltage rating devices connected in series. Also it has a potential to get a high quality output voltage by producing multi output voltage levels. However, it increases the number of switching devices and other components resulted in the increase of complexity problem and system cost.

To alleviate these problems, multilevel inverters using a cascaded transformer have been studied. In the paper, the cascade transformers produce trinary output voltage and it improves the shape of output voltage waveform. The multilevel inverter approach has merits in reduction of the number of switching devices and in a galvanic isolation between a source and loads by employing a cascaded transformer. However, it may decrease the power conversion efficiency, and increases volume and cost of the system due to the transformer. To decrease the number of transformers, a modified version of the cascaded-transformer based multilevel inverter has been reported. The presentable advantage of the method is to produce a high quality output voltage wave with reduced number of transformers. However, it still has a drawback in power conversion loss generated by usage of the transformers. To solve the problem, a modified multilevel inverter configuration has been introduced to reduce the number of independent input voltage source with minimum electric components and maximum output voltage level. The inverter is configured by two independent DC input voltage sources, two H-bridge modules, and two bidirectional switches and it produces nine output voltage levels. There are 24 basic switching patterns with the 9 output voltage levels. Among the patterns, we select 2 best efficient switching patterns to get lower switching loss and minimum *dv/dt* stress. And then we analyze characteristics of total harmonic distortion (THD) of the output voltage with variation of input voltage. To verify the performance of the selected switching patterns, we carried out simulation and experiments based on a prototype.

2 EFFICIENT SWITCHING PATTERNS FOR MODIFIERD MULTILEVEL INVERTER

In the multilevel inverter which has couple of bidirectional switches, one side of the switch is connected at neutral points of input voltages sources and the other is connected at neutral points of the H-bridge module as shown in Figure 1. To generate nine output voltage levels, it needs two independent

dc input voltage sources, two H-bridge modules, and two bidirectional switches. The circuit configuration of the proposed inverter is very similar configuration of a serial connection of conventional five-level inverters. It can prevent the efficiency drop induced by transformer in the multilevel configuration. It can reduce the number of switches compared with the conventional cascaded H-bridge multilevel inverter.

To synthesize nine output voltage levels, it employs two independent DC voltage sources of 2*E* which are divided into two input sources *E* in order to secure an additional DC voltage source of *E*. The inverter module having a bidirectional switch produce a 5-level of output voltage (-2*E*, -*E*, 0, *E*, 2*E*) by controlling of the switches. Since every output terminal of the inverter module is connected in series, the output voltage becomes the sum of the terminal voltage of each inverter.

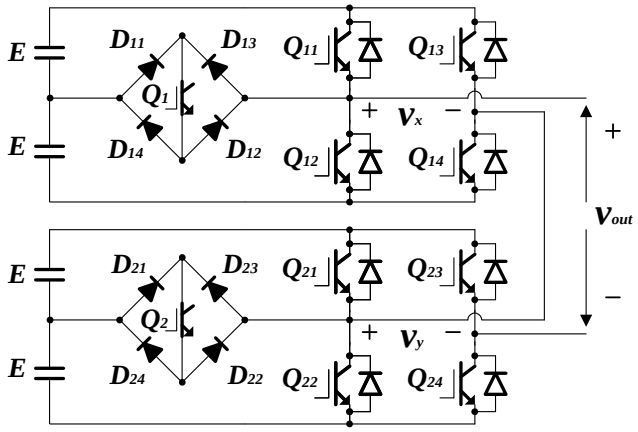


Figure 1. Circuit configuration of the proposed multilevel inverter having bidirectional switches to produce nine output voltage levels.

The switching function of an inverter can be summarized as

$$\begin{aligned} &if\ (Q_{n1}, Q_{n4}) = on \quad then \quad SF_n = 2 \\ &if\ (Q_{n}, Q_{n4}) = on \quad then \quad SF_n = 1 \\ &if\ (Q_{n1}, Q_{n3}) or (Q_{n2}, Q_{n4}) = on \quad then \quad SF_n = 0 \\ &if\ (Q_{n}, Q_{n3}) = on \quad then \quad SF_n = -1 \\ &if\ (Q_{n2}, Q_{n3}) = on \quad then \quad SF_n = -2 \end{aligned} \tag{1}$$

For generation of nine levels in an output voltage wave, we consider 24 switching patterns which are obtained by mixing the switching functions (SF_n) as listed in Table 1. It shows switching functions for generating positive output levels. By multiplying -1 to Table 1, we can obtain switching functions for a negative case.

With the switching function, output voltage of the proposed inverter is expressed in Eq. (1). The number of output voltage levels is given by Eq. (2).

$$v_{out} = \sum_{n=1}^{\infty} SF_n \cdot E \tag{2}$$

$$N = 4k + 1 \tag{3}$$

where k is the number of inverter modules. If we apply Eq. (1) for two inverter modules, v_{out} can be -4*E*, -3*E*, -2*E*, -*E*, 0, *E*, 2*E*, 3*E*, 4*E* by selecting of a proper switching pattern.

Table 1. Switching function for 9-level output voltage

No. of output levels	Switching Function		Output Voltage of each inverter		Output Voltage
	SF_1	SF_2	v_x	v_y	v_{out}
4	2	2	2E	2E	*4E*
3	2	1	2E	E	*3E*
	1	2	E	2E	
2	1	1	E	E	*2E*
	0	2	0	2E	
	2	0	2E	0	
1	0	1	0	E	*E*
	1	0	E	0	
	2	-1	2E	-E	
	-1	2	-E	2E	
0	0	0	0	0	0

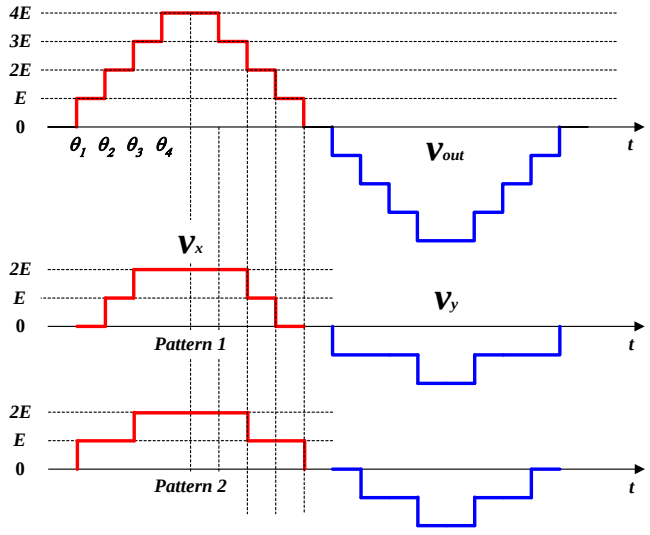
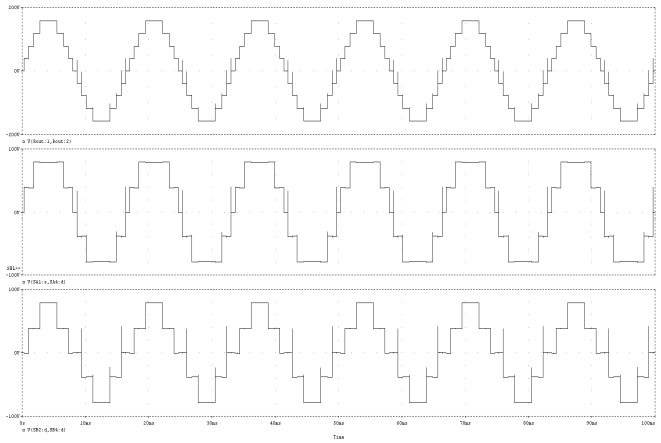


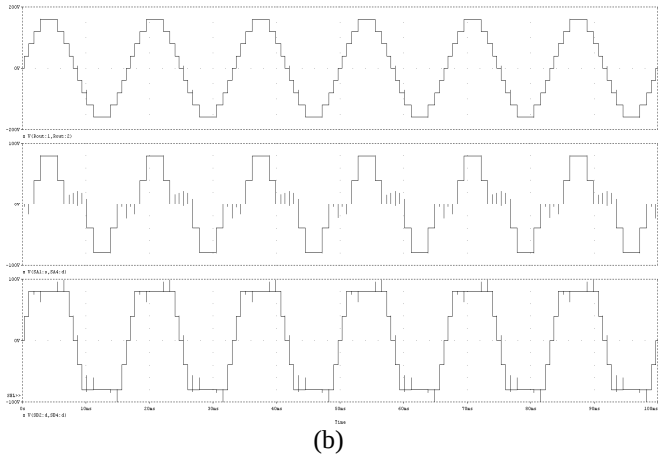
Figure 2. Switching patterns for generating a 9-level output voltage.

From Table 1, we can consider 24 switching patterns to generate a 9-level output voltage. Among them, 2 switching patterns are shown in Figure 2. It shows output patterns of upper and lower module. During the pattern selection, cross switching was avoided. That is, if the v_x indicates upper module output voltage levels with a positive polarity, then v_y should be a lower module output voltage levels with a negative polarity. Among 24 switching patterns, pattern 1 and pattern 2 have low switching times in a period. Other patterns have more switching times or have relatively higher *dv/dt* variation. Therefore we study switching pattern for the pattern 1 and 2 with simulation and experiment in this paper.

3 SIMULATION AND EXPERIMENTS



(a)



(b)

Figure 3. Simulation waveforms of output voltage (v_{out}), output voltages of the upper inverter (v_x) and the lower inverter (v_y), (a) Pattern 1, (b) Pattern 2.

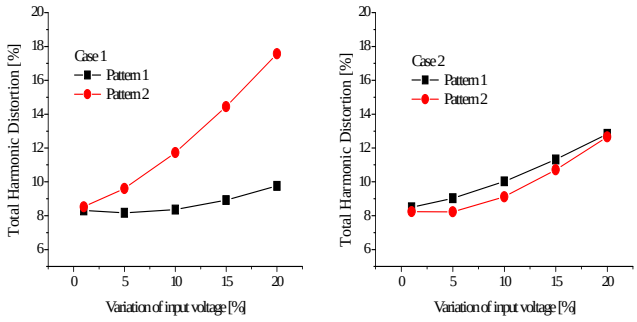
We performed computer-aided simulations for pattern 1 and 2 with the modified H-bridge multilevel inverter. The simulation was implemented by PSpice with consideration of pure resistive load. Figure 3 shows simulation waveforms of pattern 1 and 2. It shows output voltage (v_{out}), terminal voltages of the upper (v_x) and the lower (v_y) inverter in sequence. We can notice that one inverter generates a fundamental output voltage, and then another inverter adds voltages on the fundamental voltage to produce stepped waves. Consequently, the final output voltage becomes the sum of terminal voltage of H-bridge modules. Patterning difference of pattern 1 and 2 is come from output voltage's switching angle difference of the upper and lower module. If we explain the result with energy transfer, the difference of output voltage's area in upper and lower module in pattern 1 is much smaller than pattern 2's. From the Figure 3, the area of the waveform can be translated as the energy transfer from each module to the load. By simple visual comparison, we can see the area difference between upper and lower module in pattern 1 is smaller than pattern 2. The proposed multilevel inverter requires two independent input voltage sources for the upper and lower inverter module and each input voltage source is connected with two capacitors which is in series. Therefore, there is a possibility that voltages difference on the capacitors influences on the THD of the output voltages. To analysis the effect, we chose 6 cases summarized in Table 2 and executed simulations.

Table 2. Case SUMMARY: The variation of output voltage by capacitive input voltage difference

Case	Condition
1	Higher voltage on the upper module, Total input voltage: DC 160 V
2	Higher voltage on the lower module, Total input voltage: DC 160 V
3	Higher capacitive voltage cross the upper capacitor on the upper module, Input voltage on lower module: DC 80 V
4	Higher capacitive voltage cross the lower capacitor on the upper module, Input voltage on lower module: DC 80 V
5	Higher capacitive voltage cross the upper capacitor on the lower module, Input voltage on upper module: DC 80 V
6	Higher capacitive voltage cross the lower capacitor on the lower module, Input voltage on upper module: DC 80 V

Figure 4 shows variations of output voltage's THD when voltage on the upper or lower module is increased with constant DC 160 V total input voltage. When upper module voltage is higher (case 1), simulation result is shown in Figure 4(a). With the switching pattern 1, the THD variation of output voltage is less than 1 % as input voltage is changed. But, with the switching pattern 2, the THD variation of output voltage is drastically increased as much as 18 % when input voltage is changed. If we explain the result with Figure 3, the fundamental voltage

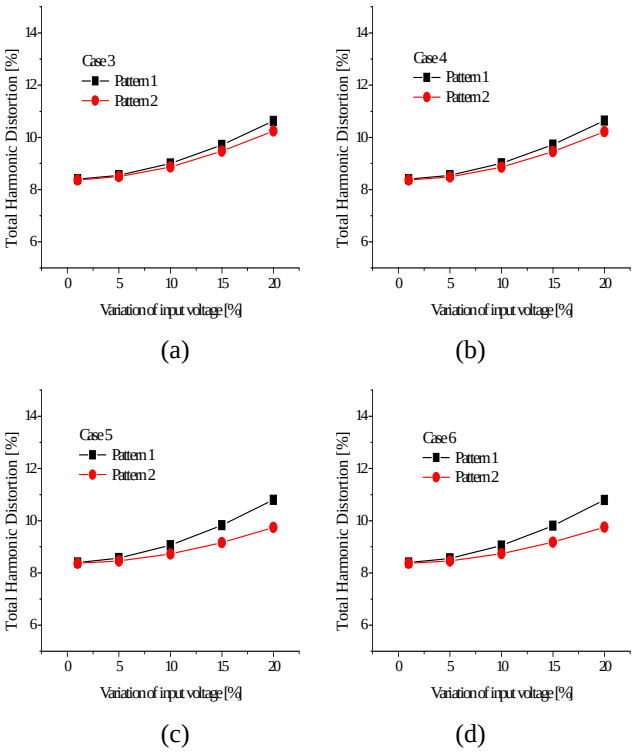
(upper module voltage in pattern 1 and lower module voltage in pattern 2) waveform is added with counterpart modules' voltage (lower module voltage in pattern 1 and upper module voltage in pattern 2) waveform to produce output voltage waveform. In the pattern 1, the fundamental and the added voltage have very similar waveform. Therefore, the THD of output voltage has little effected by the added voltage. But in the pattern 2, the fundamental voltage (lower module voltage) is a much similar waveform to the final waveform than the added voltage (upper module voltage). If we increase the voltage of the upper module voltage in pattern 2, steps between each angle on the upper level is increased. Therefore the final waveform of the output voltage in pattern 2 has bigger distortion than pattern 1. Figure 4(b) shows case 2 that is higher voltage on the lower module with constant total input voltage (DC 160V). The result shows that the THD variation of output voltage is almost same in case of pattern 1 and pattern 2. Even though voltage of the lower module in the pattern is increased, the final output voltage waveform is followed the increased lower module waveform.



(a) (b)

Figure 4. Output voltage's THD variation as capacitive input voltage is varied. (a) Case 1, (b) Case 2.

Figure 5 describes simulation results of case 3 to case 6 in Table 2. As described in previous result, when variation of the total input voltage is relatively big, the pattern 1 has better performance in the THD variation of output voltage. But, with relatively less variation of input voltage in case 3~ 6, the pattern 2 has better performance in the THD variation of output voltage. From the Figure 3, lower module of the pattern 2 is dominant waveform in production of the final output voltage waveform. With the condition of case 3~6, the input voltage variation is relatively smaller than case 1 and 2. That is, the input voltage variation has little influence to the final output voltage waveform. Therefore, the output voltage waveform in pattern 2 has a similarity to the voltage waveform in lower module which is dominant. But in the pattern 1, the waveforms in lower and upper has very similar shape.



(a) (b)

(c) (d)

Figure 5. Output voltage's THD variation as capacitive input voltage is varied, (a) Case 3, (b) Case 4, (c) Case 5, (d) Case 6.

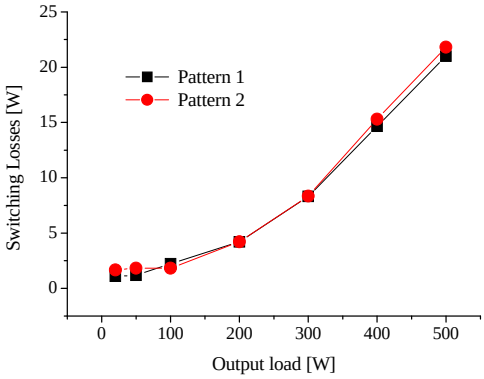


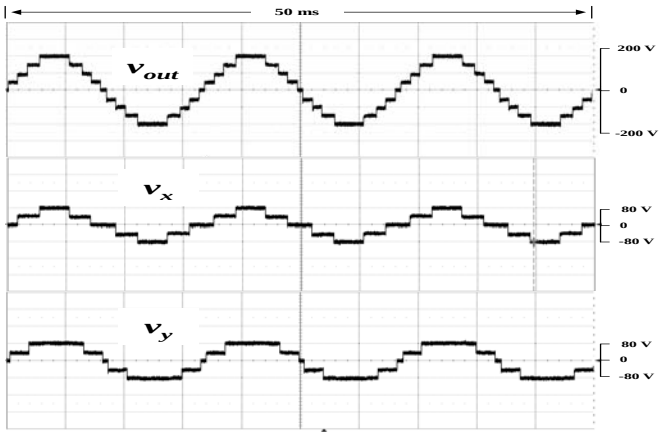
Figure 6. Switching loss comparison of pattern 1 and 2 with output load variation.

Figure 6 describes switching loss of pattern 1 and 2 with output load variation. The result shows that there is very similar switching loss, but it seems that the pattern 1 has a little better performance than pattern 2. This tiny difference seems to be generated by difference of switching angle which can produce changing of current value. From the above simulation results, the switching pattern 1 is appropriate to the proposed circuit configuration because of its better performance in switching loss, and in THD

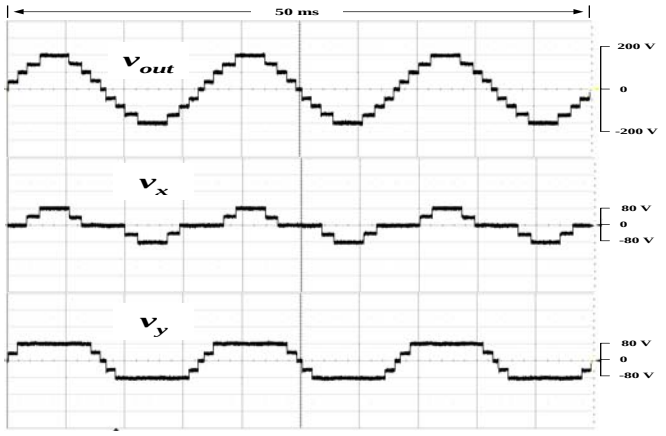
characteristic of output voltage. Also the switches in pattern 1 can have longer life time since the applied power capacity on the switches has little difference. That is, the difference in pattern 1 is smaller than one of the pattern 2.

Based on the simulation results, the proposed multilevel inverter was tested by a prototype. As a controller, AVR MEGA 128 was used. Figure 7 shows experimental waveforms of pattern 1 and 2. It includes a reference voltage, output voltage (v_{out}), terminal voltages of the upper (v_x) and the lower (v_y) inverter in sequence. The output voltage has nine levels including a zero level. Although it is close to a sinusoidal wave, it has some lower order harmonics. So it should be improved by more H-bridge modules or output filter to obtain high quality output voltages.

Figure 8 is an efficiency comparison of two switching patterns when it is applied for the proposed inverter with variation of output load from 0 to 500 W. The simulation and experimental results show that the switching pattern 1 has a little better performance in the efficiency.



(a)



(b)

Figure 7. Experimental waveforms of output voltage (v_{out}), terminal voltages of the upper inverter (v_x) and the lower inverter (v_y), (a) pattern 1, (b) pattern 2.

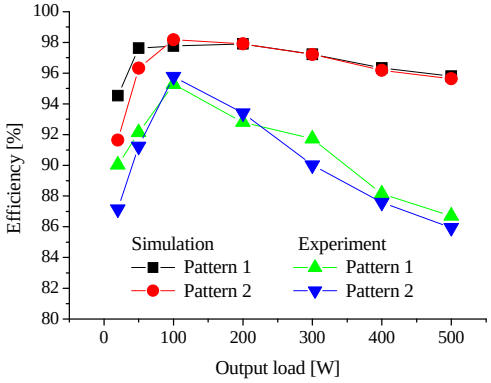


Figure 8. Efficiency comparison with the switching patterns.

From the comparison, it is clear that the most outstanding advantage of the proposed multilevel inverter scheme is the elimination of transformer in the main power stage. However, each cell of the proposed multilevel inverter requires its own isolated power supply. The provision of these isolated supplies is the main limitation in the power electronic circuit design. So the proposed multilevel inverter with the efficient switching patterns is suitable for photovoltaic power generating systems equipped with distributed power sources.

4 CONCLUSION

In the cascaded H-bridge multilevel inverter using bidirectional switches, we have selected two kinds of switching patterns among 24 possible switching patterns, which can produce a 9-level output voltage. From simulations and experiments, we claims that the proposed multilevel inverter is

(1) Economical to produce multilevel outputs by using bidirectional switches,

(2) Easy to increase of the output voltage levels and output power owing to modularity characteristic

(3) Efficient in the power management with switching pattern 1 due to its lower THD variation, longer switch lifetime and lower switching loss.

The proposed multilevel inverters can be utilized in the solar power generation which has merit in the independent voltage source

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